anabrid LUCIDAC

This is a confidential preliminary product brief for an upcoming product by anabrid. This product will be the successor of the Analog Paradigm Model-1. The project code name for the product is „LUCIDAC“.

All values are subject to change up to release.

Overview

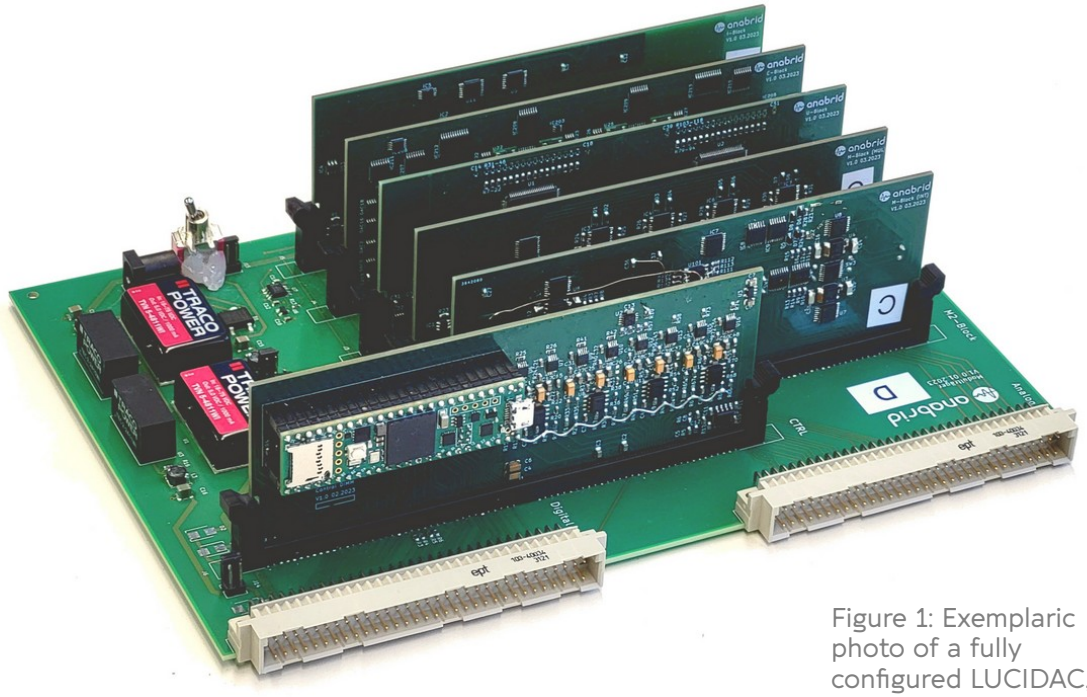

Figure 1: Exemplaric photo of a fully configured LUCIDAC, without housing.

LUCIDAC is a fully reconfigurable analog computer that serves as a co-processor for a digital computer system and is ideally suited to explore analog computing as one of the major unconventional computing paradigms.

It contains eight integrators with two selectable time-scaling factors each ($k_0 = 100$ and $k_0 = 10^4$), four multipliers, 32 coefficient elements (with 11 bits resolution and additional sign bit) and a variable number of (implicit) summers. This complement of computing elements makes it possible to solve e.g. eight coupled differential equations of 1st order or fewer with higher order, accordingly.

Using a sophisticated auto calibration system, LUCIDAC offers high precision.

LUCIDAC is equipped with the Teensy 4.1 microcontroller Unit (MCU). Communication is established by means of TCP/IP over an Ethernet interface or a serial console over USB-C port. The communication protocol is a text based JSON-lines protocol with clients for Python, C++ and Julia to be released soon. All software will be released as Open Source.

Specification

Form factor	355 x 100 x 158 mm³ (width x height x depth, including case)
Precision	Up to 12bit resolution. DC accuracy 0.1% AC bandwidth > 1Mhz (cutoff frequency).
Input power	6W (DC 24V x 250mA) Barrel jack connector, shipped with external power supply (240/120V AC Standard C13/C14).
Connectivity	Analog computing elements can be coupled all-to-all (max 32 non-zero items in 16x16 connection matrix).
Expandability	Modular design allows for future replacing computing elements, microcontroller and connection topology. Internal DIN 41612 VG-strip allows for future proof upgrades.
Product lifetime	Market launch expected end of 2023 / beginning 2024. Compatible extensions will be released in 2024.
Computing levels	The logical computing domain is $[-1,+1]$ and internally encoded in either voltages or currents. The external I/O is voltage coupled in $[-2,+2]$ V.
Ext. Connections	RJ45 for 10/100 BASE-TX Ethernet (100Mbit/sec) 16 MCX female coaxial connectors for Analog I/O 2x25 IDC header with latches for Digital I/O for use with standard flat cables. 8x LEDs for system status (four user controllable) 3x MCX trigger output (for IC/OP/Overload detection) USB-C for backup serial console and flashing (USB2) For a preliminary diagram, see below.

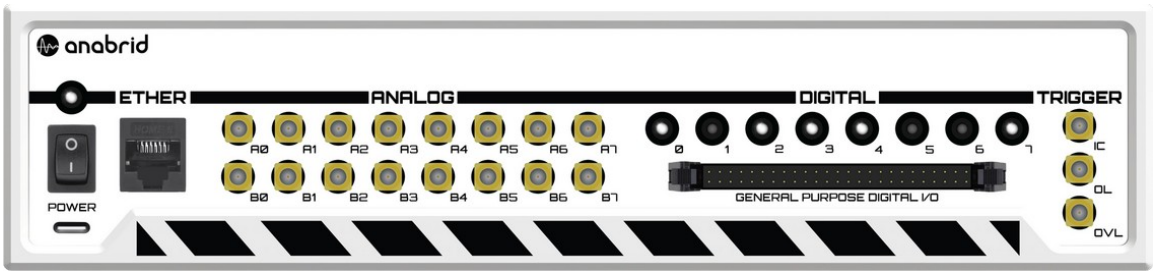

Figure 2: Preliminary working draft design of the front panel. Note the yellow MCX sockets and the pin header for digital I/O.

Analog Computing Elements

Integrators

Each integrator computes the time integral over an input signal (which can itself be the sum of several variables) and can be initialised to any value within $[-1,1]$. There are two software selectable time-scale factors $k_0 \in \{100, 10^4\}$ which allow for a wide range of scaling.
Offset and linearity errors are compensated for using the auto calibration feature of the system.
In addition to this, each integrator features a configurable upper and lower limiter, making it easy to implement non-linear systems, hard limits etc.

Multipliers

Each multiplier computes the product of two input variables.
Offset errors of the multipliers are compensated for using the auto calibration feature of the system.

Coefficient elements

In a LUCIDAC there are 32 coefficient elements each capable of setting a parameter in the interval $[-1,+1]$ in a program. These are implemented using multiplying DACs (Digital-Analog-Converters).

Connectivity

All computing elements of a LUCIDAC system can be freely connected with each other using anabrid's novel interconnect architecture. At its heart are several electronic crossbar switches.
The architecture allows for 8 external analog outputs and 8 external analog inputs, furthermore a general purpose digital I/O pin header allows for connecting custom digital equipment with low latency to the MCU.

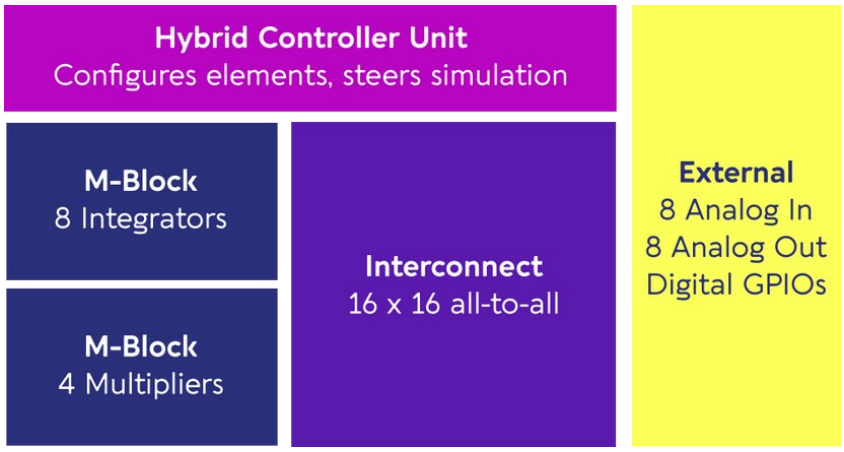

Figure 3: Overview logical block picture of the LUCIDAC.

Digital Hardware and Software

Data Aquisition

Data acquisition: Since results of an analog computation are time variable signals, LUCIDAC allows capture of up to eight analog variables at up to 500.000 samples per second (SPS). Thus, every detail of an analog computation can be retrieved without the need for external measurement devices.

Microcontroller

The integrated Teensy Microcontroller runs firmware provided by anabrid which allows for steering the analog simulation. Advanced users can program adopt the firmware to write sophisticated analog-digital hybrid programs with minimal latency. On-air scripting will be provided to simplify this process as much as possible. The firmware and communication protocol will be open sourced as well as the reference client implementation in Python and other languages such as C++ and Julia.

Software examples

The following code snippet shows how LUCIDAC computing elements can be configured on a low-level base:

```
# Set alias for cluster
set-alias * carrier
set-alias carrier/0 cluster
set-alias cluster/M0/0 osc_x

# Configure routing on cluster
route -- cluster 8 0 1.0 9
route -- cluster 9 1 -1.0 8
set-element-config osc_x ic 0.71
set-connection cluster/U 8 8
set-connection cluster/U 9 9

# Start run
run
```

Further and more complex programming examples will be released soon.

For further information contact our engineering team at hello@anabrid.com.

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